REMARKS

This Application has been carefully reviewed in light of the Final Office Action mailed January 11, 2006 ("Office Action"). At the time of the Office Action, Claims 1-21 were pending in the application. In the Office Action, the Examiner rejects Claims 1-21. Applicant respectfully requests reconsideration and allowance of all pending claims.

Claim Rejections - 35 U.S.C. § 102

The Examiner rejects Claims 1-21 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,826,013 issued to Nachenberg (*"Nachenberg"*). Applicant respectfully requests reconsideration and allowance of Claims 1-21.

Nachenberg fails to support the rejection of Claim 1 for at least two reasons. First, the cited reference fails to teach, suggest, or disclose "an exception handler or an interrupt handler" as recited, in part, in Claim 1. Second, *Nachenberg* fails to teach, suggest, or disclose that "the at least one modification...comprises installation of an exception handler or an interrupt handler" as recited, in part, in Claim 1.

First, the cited reference fails to teach, suggest, or disclose "an exception handler or an interrupt handler" as recited, in part, in Claim 1. With respect to "an exception handler" recited in Claim 1, the Examiner states: "The common definition of the term is that an exception handler is a section of code which defines the recovery actions to be performed in response to exceptions raised within that code." (Office Action; p. 2). The Examiner cites nothing in support of this statement. Accordingly, Applicant traverses the Examiner's reliance on common knowledge. There is simply nothing in *Nachenberg* that teaches, suggests, or discloses "an exception handler or an interrupt handler" as recited, in part, in Claim 1. To maintain the rejection of Claim 1, the Examiner must provide documentary evidence or an affidavit or declaration in support of the Examiner's foregoing statement regarding the "common definition" of an exception handler. MPEP § 2144.03(C). Otherwise, the rejection of Claim 1 must be withdrawn.

Second, *Nachenberg* fails to teach, suggest, or disclose that "the at least one modification...comprises installation of an exception handler or an interrupt handler" as recited, in part, in Claim 1. In analyzing "the at least one modification" recited in Claim 1, the Examiner cites a portion of *Nachenberg* that describes detecting "non-initialized indexed writes" and determining whether an "index register has been initialized or modified."

(*Nachenberg*; col. 12, ll. 65-66; col. 13, ll. 3-5). Thus, the Examiner seems to equate the non-initialized indexed writes and the modified index register in *Nachenberg* with "the at least one modification" recited in Claim 1. Notably, however, *Nachenberg* fails to teach, suggest, or disclose that the non-initialized indexed writes and the modified index registers comprise installation of anything. (*Nachenberg*; col. 12, ll. 65-66; col. 13, ll. 3-5). Thus, the cited reference fails to teach, suggest, or disclose that "the at least one modification...comprises *installation* of an exception handler or an interrupt handler" as recited, in part, in Claim 1. (Emphasis added). The Examiner cites another portion of *Nachenberg* that describes interrupting an emulation process. (*Nachenberg*; col. 4, ll. 25-29). In particular, the cited reference describes a module that "tracks those parts of virtual memory modified during emulation and periodically interrupts the emulation process to call the scanning module." (*Nachenberg*; col. 4, ll. 25-29). Notably, however, merely interrupting an emulation process has nothing to do with "*installation* of an exception handler or an interrupt handler" as recited, in part, in Claim 1. (Emphasis added). There is simply nothing in *Nachenberg* that teaches, suggests, or discloses that "the at least one modification...comprises installation of an exception handler or an interrupt handler" as recited, in part, in Claim 1. It is well established that a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). In addition, "[t]he identical invention *must* be shown in as complete detail as is contained in the...claim," and "[t]he elements *must* be arranged as required by the claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989); *In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990); MPEP § 2131 (emphasis added). Because *Nachenberg* fails to teach, suggest, or disclose that "the at least one modification...comprises installation of an exception handler or an interrupt handler" as recited in Claim 1, the rejection is improper. For at least these reasons, Applicant respectfully requests reconsideration and allowance of Claim 1.

In rejecting Claims 8-11, the Examiner employs rationale that is analogous to that used in rejecting Claim 1. Accordingly, for reasons analogous to those stated with respect to Claim 1, Applicant respectfully requests reconsideration and allowance of Claims 8-11.

Claims 2-7 and 12-21 depend from independent claims shown above to be allowable. In addition, these claims recite further elements not taught, suggested, or disclosed by the

cited references. First, *Nachenberg* fails to teach, suggest, or disclose "instructions for forcing a corresponding exception" as recited, in part, in Claim 2. Second, *Nachenberg* fails to teach, suggest, or disclose "detecting writing of a pointer to at least one predetermined address in a system memory for storing an exception handler pointer" as recited, in part, in Claim 3. Third, the cited reference fails to teach, suggest, or disclose that "access to the second memory component is more restricted than access to the first memory component" as recited, in part, in Claim 20. Fourth, the cited reference fails to teach, suggest, or disclose that "the exception handler or the interrupt handler attempts to modify the second memory component" as recited, in part, in Claim 21.

First, *Nachenberg* fails to teach, suggest, or disclose "instructions for forcing a corresponding exception" as recited, in part, in Claim 2. In rejecting Claim 2, the Examiner cites a portion of *Nachenberg* that describes a module that emulates file instructions, "tracks those parts of virtual memory modified during emulation and periodically interrupts the emulation process to call the scanning module." (*Nachenberg*; col. 4, ll. 23-31). Thus, the cited reference discloses a module that periodically interrupts the emulation process. However, merely interrupting an emulation process does not teach, suggest, or disclose "a corresponding exception" as recited, in part, in Claim 2. In addition, interrupting an emulation process does not teach, suggest, or disclose that "the emulated computer executable code *comprises instructions for forcing* a corresponding exception" as recited, in part, in Claim 2. (Emphasis added). Because the cited reference fails to teach, suggest, or disclose this aspect of Claim 2, the cited reference does not support the rejection.

Second, *Nachenberg* fails to teach, suggest, or disclose "detecting writing of a pointer to at least one predetermined address in a system memory for storing an exception handler pointer" as recited, in part, in Claim 3. In rejecting Claim 3, the Examiner cites a portion of *Nachenberg* that describes emulating file instructions. In particular, the cited portion states: "Register-indirect memory write instructions write data to a memory address specified by a pointer register." (*Nachenberg*; col. 3, ll. 54-59). Merely determining an address specified by a pointer register, however, does not teach, suggest, or disclose "writing of a pointer" as recited, in part, in Claim 3. In addition, the cited reference only discloses that "the pointer register is typically the index (SI or ESI) register." (*Nachenberg*; col. 3, ll. 56-57). This statement does not teach, suggest, or disclose "storing *an exception handler pointer*" as recited, in part, in Claim 3. (Emphasis added). As a result, *Nachenberg* fails to teach,

suggest, or disclose "detecting writing of a pointer to at least one predetermined address in a system memory for storing an exception handler pointer" as recited, in part, in Claim 3. Because the cited reference fails to teach, suggest, or disclose this aspect of Claim 3, the cited reference does not support the rejection.

Third, the cited reference fails to teach, suggest, or disclose that "access to the second memory component is more restricted than access to the first memory component" as recited, in part, in Claim 20. In rejecting Claim 20, the Examiner cites the Abstract and Figure 2 of *Nachenberg*. The Abstract and Figure 2 disclose numerous components, including an emulator, an emulation control module, a scanning module, a static exclusion module, a table, file types, and virus signatures. (*Nachenberg*; Abstract). The Examiner fails to identify which of these components he equates with "the first memory component" and which of these components he equates with "the second memory component" recited in Claim 20. It is well established that "[w]hen a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable." 37 C.F.R. § 1.104(c)(2). With respect to Claim 20, the Examiner's conclusory statement regarding the purported teachings of *Nachenberg* does not comply with the requirements of 37 C.F.R. § 1.104(c)(2). Therefore, the rejection of Claim 20 is improper. Applicant further submits that nothing in the cited portion of *Nachenberg* teaches, suggests, or discloses that "access to the second memory component *is more restricted* that access to the first memory component" as recited, in part, in Claim 20. (Emphasis added). Because the cited reference fails to teach, suggest, or disclose this aspect of Claim 20, the cited reference fails to support the rejection.

Fourth, the cited reference fails to teach, suggest, or disclose that "the exception handler or the interrupt handler attempts to modify the second memory component" as recited, in part, in Claim 21. As shown above, the Examiner fails to identify which component of *Nachenberg* he equates with the "second memory component" recited in Claim 21. Consequently, the rejection of Claim 21 is improper. Applicant submits that nothing in the portion of *Nachenberg* cited by the Examiner teaches, suggests, or discloses that "the exception handler or the interrupt handler attempts to modify the second memory component" as recited, in part, in Claim 21. Because the cited reference fails to teach, suggest, or disclose this aspect of Claim 20, the cited reference fails to support the rejection.

For at least the foregoing reasons, Applicant respectfully requests reconsideration and allowance of Claims 2-7 and 12-21.

CONCLUSION

Applicant has made an earnest attempt to place this case in condition for allowance. For the foregoing reasons, and for other reasons clearly apparent, Applicant respectfully requests full allowance of all pending claims.

If the Examiner feels that a telephone conference would advance prosecution of this Application in any manner, the Examiner is invited to contact Samir A. Bhavsar, Attorney for Applicant, at the Examiner's convenience at (214) 953-6581.

The Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

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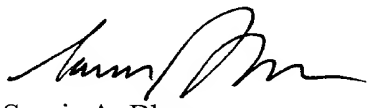

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